IN THE CLAIMS:

Claim 1 (Currently Amended): A test pattern for measuring a contact resistance, comprising:

a test wafer in which a plurality of device isolation ~~films~~ structures are formed to define a plurality of active regions;

a plurality of interconnection diffusion layers formed in a word line region crossing the plurality of device isolation ~~films~~ structures and the plurality of active regions;

a plurality of source diffusion layers formed in a first line contact region located at a first side of the word line region;

a plurality of source diffusion layers formed in a second line contact region located at a second side of the word line region; and

a plurality of line contact patterns formed in the first and second line contact regions,

wherein the line contact patterns formed in the first line contact region and the line contact patterns formed in the second line contact region are alternately positioned, and current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in three dimensions.

Claim 2 (Previously Presented) The test pattern according to claim 1, wherein the word line region, the first line contact region, and the second line contact region are juxta-positioned.

Claim 3 (Previously Presented): The test pattern according to claim 1, wherein the source diffusion layer in the first line contact region and the source diffusion layer in the second line contact region are electrically connected by an interconnection diffusion layer in the word line region.

Claim 4 (Currently Amended): The test pattern according to claim 1, wherein one of the plurality of line contact patterns in the first line contact region electrically connects two of the plurality of source diffusion layers in the first line contact region and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 5 (Currently Amended): The test pattern according to claim 1, wherein one of the plurality of line contact patterns in the second line contact region electrically connects two of the plurality of source diffusion layers in the second line contact region, and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 6 (Currently Amended) : A method of manufacturing a test pattern for measuring a contact resistance, comprising:

forming a plurality of device isolation ~~films~~ structures in a test wafer to define a plurality of active regions;

simultaneously forming a plurality of source diffusion layers in ones of the plurality of active regions of a first line contact region, a plurality of interconnection diffusion layers in ones of the plurality of active regions of a word line, and a plurality of source diffusion layers in ones of the plurality of active regions of a second line contact region;

forming a word line surrounded by an insulating film spacer in the word line region;

forming an insulating layer on an entire structure including the word line, the insulating layer having a flattened surface;

forming a self-aligned contact mask on the insulating layer; and

forming a plurality of line contact patterns in the first and second line contact regions through a self-aligned contact process using the self-aligned contact mask,

wherein the line contact pattern formed in the first line contact region and the line contact pattern formed in the second line contact region are alternatingly positioned, and current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in three dimensions.

Claim 7 (Currently Amended): The method according to claim 6, wherein the word line region, the first line contact region, and the second line contact region are juxta-positioned crossing the plurality of device isolation ~~films~~ structures and the plurality of active regions.

Claim 8 (Previously Presented): The method according to claim 6, wherein one of the plurality of source diffusion layers in the first line contact region and one of the plurality of the source diffusion layers in the second line contact region are electrically connected by one of the plurality of interconnection diffusion layers in the word line region.

Claim 9 (Currently Amended): The method according to claim 6, wherein one of the plurality of line contact patterns in the first line contact region electrically connects two of the plurality of source diffusion layers in the first line contact region and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 10 (Currently Amended): The method according to claim 6, wherein one of the plurality of line contact patterns in the second line contact region electrically connects two of the plurality of source diffusion layers in the second line contact region, and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 11 (Currently Amended): The method according to claim 6, wherein the self-aligned contact mask is formed to cover an upper portion of the word line, an upper portion of the device isolation ~~film~~ structure between a first one of the plurality of source diffusion layers and a second one of the plurality of source diffusion layers in the first line contact region, and an upper portion of the device isolation ~~film~~ structure between the second one of the plurality of source diffusion layers and a third one of the plurality of source diffusion layers in the second line contact region.

Claim 12 (Currently Amended): A method of manufacturing a test pattern for measuring a contact resistance, comprising:

forming a plurality of device isolation ~~films~~ structures in a test wafer to define a plurality of active regions;

forming ~~a threshold voltage~~ an ion implantation region in the plurality of active regions in a word line region to form a channel for controlling a threshold voltage;

forming a word line in the word line region;

forming a plurality of source diffusion layers in each of the plurality of active regions of a first line contact region;

forming a plurality of source diffusion layers in each of the plurality of active regions of a second line contact region;

forming an insulating film spacer surrounding the word line;

forming an insulating layer on an entire structure including the word line, the insulating layer having a flattened surface;

forming a self-aligned contact mask on the insulating layer; and

forming a plurality of line contact patterns in the first and second line contact regions through a self-aligned contact process using the self-aligned contact mask,

wherein the line contact pattern formed in the first line contact region and the line contact pattern formed in the second line contact region are alternatingly positioned, and current for measuring a resistance flows along the first line contact region and the second line contact region between the word line in three dimensions.

Claim 13 (Currently Amended): The method according to claim 12, wherein the word line region, the first line contact region, and the second line contact region are juxta-positioned crossing the plurality of device isolation ~~films~~ structures and the plurality of active regions.

Claim 14 (Currently Amended): The method according to claim 12, wherein the plurality of source diffusion layers in the first line contact region and the plurality of source diffusion layers in the second line contact region are electrically connected by ~~a channel formed in the threshold voltage ion-implantation region by applying a voltage to the word line~~ the ion implanation region in the word line region.

Claim 15 (Currently Amended): The method according to claim 12, wherein one of the plurality of line contact patterns in the first line contact region electrically connects two of the plurality of source diffusion layers in the first line contact region, and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 16 (Currently Amended): The method according to claim 12, wherein one of the plurality of line contact patterns in the second line contact region electrically connects two of the plurality of source diffusion layers in the second line contact region, and is ~~electrically isolated from~~ alternately positioned with another one of the plurality of line contact patterns.

Claim 17 (Currently Amended): The method according to claim 12, wherein the self-aligned contact mask is formed to cover an upper portion of the word line, an upper portion of the device isolation ~~film~~ structure between a first one of the plurality of source diffusion layers and a second one of the plurality of source diffusion layers in the first line contact region, and an upper portion of the device isolation ~~film~~ structure between the second one of the plurality of source diffusion layers and a third one of the plurality of source diffusion layers in the second line contact region.